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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/046,497	10/26/2001	Er-Xuan Ping	MTI-31041-A	8624

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EXAMINER
LE, THAO X

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 04/10/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/046,497	Applicant(s) PING ET AL.	
	Examiner Thao X Le	Art Unit 2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *101-116,123-223* is/are pending in the application.

4a) Of the above claim(s) 161-164 is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *101-116,123-135, 137-160, and 165-223* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

1. Claims 101-102, 106-109, 194, 196-223 are rejected under 35 U.S.C. 102(e) as being anticipated by US 6232641 Miyano et al.

Regarding to claim 101, Miyano discloses a transistor in a semiconductor device fig. 6K comprising, source/drain (S/D) diffusion regions 14/15 formed on the semiconductive region of a substrate 1, the transistor gate 7 formed on the semiconductive region between the S/D diffusion regions 14/15, the transistor gate extending in a vertical orientation from the substrate 1, the transistor gate comprising at least two overlying layers (7/12) of epitaxial silicon, including an uppermost epitaxial layer 12, columns 10 line 17 and column 11 lines 5, each epitaxial silicon

layer comprising a top surface and insulated sidewalls 11, the uppermost epitaxial silicon layer having an insulated top surface 17.

Regarding to claims 102, 106-109, Miyano discloses a transistor in a semiconductor device fig. 6K comprising wherein source/drain (S/D) diffusion regions 16 are elevated, wherein the epitaxial comprises a facet top surface, column 10 line 65, having a thickness of about 50 nm to 200 nm, column 11 line 10, having a oxide isolation structure 3, fig. 6K

Regarding to claim 194, Miyano discloses a transistor in a semiconductor device fig. 6K comprising, source/drain (S/D) diffusion regions 14/15 disposed on the semiconductive region of a substrate 1, the transistor gate 7 disposed on the semiconductive region between the S/D diffusion regions 14/15, the transistor gate extending in a vertical orientation from the substrate 1, the transistor gate comprising at least two overlying layers (7/12) of epitaxial silicon, wherein a fist epitaxial layer 7 is disposed on the substrate, and the second epitaxial Si layer 12 is disposed on the top surface of the first epitaxial Si layer 7, and an uppermost epitaxial layer 12, columns 10 line 17 and column 10 lines 5, each epitaxial silicon layer comprising a top surface and insulated sidewalls 11, the uppermost epitaxial silicon layer having an insulated top surface 17.

Regarding to claims 196-223, as discussed in claim 194 above, Miyano discloses all the limitations of claims 196-222 including dopant, column 11 line 26, sidewall 11, being a transistor.

The process limitations "removing, selectively grow, repeating, etc.." in claim 203-223, do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

1. Claims 101-116, 123-130, 132-135, 137-160, 165-223 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 5397909 to Moslehi in view of US 5902125 to Wu

Regarding to claim 101, Moslehi discloses a transistor in a semiconductor device fig. 19 comprising, source/drain (S/D) diffusion regions 64 formed on the semiconductive region of a substrate 38, the transistor gate 88 formed on the semiconductive region between the S/D diffusion regions 64, the transistor gate extending in a vertical orientation from the substrate 20, the transistor gate comprising at least two overlying layers (50/88) of epitaxial silicon, including an uppermost epitaxial layer 88, columns 14 line 17 and column 18 lines 10-20, each epitaxial silicon layer comprising a top surface and insulated sidewalls 60.

But Moslehi reference does not expressly disclose a transistor gate wherein an uppermost epitaxial silicon layer having an insulated top surface. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Moslehi's device and apply the insulator on the top surface of the epitaxial layer as claim, because such insulator layer is conventional in the art either to protect the silicon layer or for further connection, see Wu, fig. 8.

Regarding to claims 102, 104-108, 111-115, 124-128, 130, 132-135, 137-147, 150-160, 165-172, 174-175, 177-178, 180-181, 183-185, 187-189, 191-193, Moslehi discloses the transistor wherein the S/D diffusion regions 87 are elevated and extend in a vertical orientation from the substrate adjacent to the transistor gate 50/88, fig. 9, wherein each epitaxial silicon layers of S/D epitaxial silicon layer comprises a conductivity enhancing dopant, fig. 17 column 18 lines 18 and 58, having a facet top surface, wherein each epitaxial silicon layer has the thickness of about 50 nm to about 200nm, column 11 line 41, column 18 line 10, wherein the transistor is isolated by a oxide dielectric isolation trench 42, column 11 line 7, n-type doping, column 13 line 37, disposed adjacent to gate, disposed adjacent to S/D, begin a transistor, being a S/D region, component of transistor, being a transistor gate, fig. 19.

With respect to p-type doping, it is conventional in the art to create PMOS.

With respect to oxide insulative material, Wu reference discloses the oxide 26, column 5 line 15. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Moslehi's device and apply the insulator on the top surface of the epitaxial layer as claim, because such insulator layer is conventional in the art either to protect the silicon layer or for further connection. With

respect to SiN, replacing SiO with SiN would have been considered a mere substitution of art-recognized equivalent values.

With respect to the thickness silicon oxide film, Wu reference discloses a thick oxide 26, column 5 line 15. Accordingly, it would have been obvious to one of ordinary skill in art to use or combine (teaching of second reference) in the range as claimed, because it has been held that where the general conditions of the claims are discloses in the prior art, it is not inventive to discover the optimum or workable range by routine experimentation. See In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955).

With respect to gradient concentration, see column 13 line 45-65 of Moslehi.

Regarding to claim 103, 116, Moslehi reference does not expressly disclose a transistor gate wherein an uppermost epitaxial silicon layer having an insulated top surface.

At the time the invention was made; it would have been obvious to one of ordinary skill in the art to use the teaching of Moslehi's device and apply the insulator on the top surface of the epitaxial layer as claim, because such insulator layer is conventional in the art either to protect the silicon layer or for further connection, see Wu (5902125).

Regarding to claim 110, 123, 129, 143, 149, 173, 176, 179, 182, 186, 190, 194-223 as discussed in the above claims 101-109, Moslehi discloses all the limitations of claims 110, 123, 129, 143, 149, 173, 176, 179, 182, 186, 190, 194-223.

The process limitations "removing, selectively grown, repeating, prior to...etc. " in claims 203-223, do not carry weight in a claim drawn to structure. In re Thorpe, 277 USPQ 964 (Fed. Cir. 1985).

2. Claim 131 is rejected under 35 U.S.C. 103(a) as being unpatentable over US 5397909 to Moslehi in view of US 5963822 to Saihara et al.

Regarding to claim 131, Moslehi does not expressly disclose the facet has a (100) plane orientation.

However, a silicon substrate would have having a plane orientation of (100) or (111) as discloses by Saihara. At the time of the invention was made, it would have been obvious to one of ordinary skill in the art to form an epitaxial layer of Moslehi having a plane orientation of (100), because such orientations are conventional and common for monocrystalline silicon substrate.

3. Claims 103-104, 110 are rejected under 35 U.S.C. 103(a) as being unpatentable over US 6232641 to Miyano et al. in view of US 6051473 to Ishida et al.

Regarding to claim 103, 110, Miyano discloses a transistor in a semiconductor device fig. 6K comprising: a transistor gate 7 disposed on the semiconductive region of the substrate 1, and elevated S/D 16 disposed on the semiconductive region adjacent to the transistor gate 7 extending in a vertical orientation from the substrate 1, and the S/D regions comprises one epitaxial silicon 12 having a top surface, and insulated sidewalls, and an uppermost epitaxial silicon layer 12 having an insulated top surface.

But, Miyano does not disclose the transistor wherein the S/D regions comprise at least two overlaying layers of epitaxial silicon.

However, Ishida reference discloses a transistor in fig. 2 wherein the S/D regions comprise at least two overlaying layers of epitaxial silicon 250 and 260. At the time the invention was made; it would have been obvious to one of ordinary skill in the art to

combine the two layers S/D regions teaching of Ishida with Miyano, because it would have suppress hot carrier injection and lower sheet and contact resistance as taught by Ishida, column 2 lines 5-12.

Regarding to claim 104, 111-116, Miyano discloses the transistor wherein the epitaxial layer 12 of S/D regions comprises conductivity enhancing dopant, column 11 line 26, wherein the epitaxial comprises a facet top surface, column 10 line 65, having a thickness of about 50 nm to 200 nm, column 11 line 10, having a oxide isolation structure 3, fig. 6K, having at least two overlaying layers of epitaxial silicon 7/12, fig. 6K.

Regarding to claim 124, 195, as discussed in claims 110-116 above, Miyano and Ishida discloses all the limitations of claims 124,

Response to Arguments

4. Applicant's arguments with respect to claims101-193 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thao X Le whose telephone number is 703-306-0208. The examiner can normally be reached on M-F from 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael M Fahmy can be reached on 703-308-4918. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722 for regular communications and 703-308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Thao X. Le
April 3, 2003

PHAT X. CAO
PRIMARY EXAMINER